REMARKS

This paper is submitted in response to the non-final Office Action mailed on November 13, 2006. Claims 16-27 are pending and Claims 16, 20, 25 and 26 are amended. No new matter is introduced by these amendments. The Commissioner is hereby authorized to charge deposit account 02-1818 for any fees which are due and owing or to credit any overpayment.

The Office Action rejected all of the claims under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,734,568 ("Watanabe I") and/or U.S. Patent No. 4,849,614 ("Watanabe II"). Applicants respectfully disagree.

Watanabe I discloses an IC card that includes a memory area in which the record length and number of records is retained as index information. The index information also includes a security level defining what is necessary to access the records. However, it is respectfully submitted that Wantanabe I does not disclose or suggest any correspondence between the size of the index and the size of a block unit of the memory area. To the contrary, Wantanabe I discloses memory areas (the size of which bears no relation to the size of the index area), records (the size of which bears no relation to the size of the index area) and bits or bites (the size of which bears no relation to the size of the index area). For at least this reason, it is respectfully submitted that Wantanabe I does not disclose or suggest that the second area includes a plurality of user blocks managed in a block unit having a predetermined size, wherein each of the plurality of area definition blocks has the predetermined size as in Claim 16.

For at least the above reasons, it is respectfully submitted that Claim 16 and its dependent claims are each patentably distinguished from Watanabe I and are in condition for allowance. For similar reasons, it is respectfully submitted that Claims 20, 25 and 26 and their respective dependent claims are each patentably distinguished from Watanabe I and are in condition for allowance.

Similarly, Watanabe II discloses a composite IC card that includes an index area in which predesignated bytes (i.e., the 6^{th} and 7^{th} bytes, respectively) identify the record length and number of records available in a storage area. Further, the index area also includes a security level defining what is necessary to access the records. However, it is respectfully submitted that, like Wantanabe I, Wantanabe II does not disclose or suggest

any correspondence between the size of the index area and the size of a block unit of the storage area. To the contrary, Wantanabe II discloses storage areas (the size of which bears no relation to the size of the index area), records (the size of which bears no relation to the size of the index area) and bits or bites (the size of which bears no relation to the size of the index area). For at least this reason, it is respectfully submitted that Wantanabe II does not disclose or suggest that the second area includes a plurality of user blocks managed in a block unit having a predetermined size, wherein each of the plurality of area definition blocks has the predetermined size as in Claim 16.

For at least this reason, it is respectfully submitted that Claim 16 and its dependent claims are each patentably distinguished from Watanabe II and are in condition for allowance. For similar reasons, it is respectfully submitted that Claims 20, 25 and 26 and their respective dependent claims are each patentably distinguished from Watanabe II and are in condition for allowance.

For the foregoing reasons, Applicants respectfully submit that the present application is in condition for allowance and earnestly solicit reconsideration of same.

Respectfully submitted,

BELL, BOYD & LLOYD LLP

BY _____

Thomas C. Basso
Reg. No. 46,541
Customer No. 29175

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